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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,084	12/23/2004	Heiji Watanabe	Q85504	7332

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
CHIU, TSZ K	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
01/21/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

sughrue@sughrue.com
PPROCESSING@SUGHRUE.COM
USPTO@SUGHRUE.COM

Office Action Summary	Application No.	Applicant(s)	
	10/519,084	WATANABE ET AL.	
	Examiner	Art Unit	
	Tsz K. Chiu	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-39* is/are allowed.

6)☒ Claim(s) *21-28 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21-24, 26-28 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Cho (the article titled "Novel Nitrogen Profile Engineering for Improved TaN/HfO2/Si MOSFET Performance" submitted in the Information Disclosure Statement filed on December 23, 2004).

As to independent claim 21, Cho discloses a semiconductor device (see the entire article, including Table 1's "Top Nitrided (TN)" transistor disclosure) comprising: a gate insulating film (the nitrogen-containing HfO2 film) and a gate electrode (the TaN or poly-Si film) stacked in this order [on a silicon substrate]; wherein said gate insulating film and said gate electrode are in contact with each other; and wherein said gate insulating film (the nitrogen-containing HfO2 film) comprises a nitrogen containing high-dielectric-constant insulating film which has a structure in which nitrogen is introduced into metal oxide or metal silicate; and the nitrogen concentration in said nitrogen containing high-dielectric-constant insulating film has a distribution in the direction of the film thickness (i.e., there is nitrogen only in the top of the HfO2 film, just like the nitrogen concentration distribution in the applicant's Fig. 1 layer 103); and a position at which the nitrogen concentration in said nitrogen containing high-dielectric constant insulating film

reaches a maximum in the direction of the film thickness is present in a region at a distance from the silicon substrate (again, there is nitrogen only at the top of the HfO2 film, just like the nitrogen concentration distribution in the applicant's Fig. 1 layer 103).

Claim 21 is thus rejected under 35 USC 102(b) as being anticipated by Cho.

As to independent claim 40, Cho discloses a semiconductor device (see the entire article, including Table 1's "Top Nitrided (TN)" transistor disclosure) comprising: a gate insulating film (the nitrogen-containing HfO2 film) and a gate electrode (the TaN or poly-Si film) stacked in this order [on a silicon substrate]; wherein said gate insulating film and said gate electrode are in contact with each other; and wherein said gate insulating film (the nitrogen-containing HfO2 film) contains nitrogen and metal oxide or metal silicate; and the nitrogen concentration in said gate insulating film has a distribution in the direction of the film thickness (i.e., there is nitrogen only in the top of the HfO2 film, just like the nitrogen concentration distribution in the applicant's Fig. 1 layer 103); and a position at which the nitrogen concentration in said gate insulating film reaches a maximum in the direction of film thickness is present in a region at a distance from the silicon substrate (again, there is nitrogen only at the top, just like the nitrogen concentration distribution in the applicant's Fig. 1 layer 103).

Claim 40 is thus rejected under 35 USC 102(b) as being anticipated by Cho.

With respect to claim 22, Cho discloses wherein a position at which the nitrogen concentration in said nitrogen containing high-dielectric-constant insulating film (the nitrogen-containing HfO2 film) reaches a maximum in the direction of the film thickness is present in a region at a distance of not less than 0.5 nm from the silicon substrate

(again, there is nitrogen only at the top of the HfO2 film, just like the nitrogen concentration distribution in the applicant's Fig. 1 layer 103).

With respect to claim 23-24, Cho discloses wherein a position at which the nitrogen concentration in said nitrogen containing high-dielectric-constant insulating film (the nitrogen-containing HfO2 film) reaches a maximum in the direction of the film thickness is localized on the side of a gate electrode (the TaN or poly-Si film) in said nitrogen containing high-dielectric-constant insulating film.

With respect to claim 26, Cho discloses wherein said gate insulating film (the nitrogen-containing HfO2 film) comprises a silicon oxide film (second paragraph of introduction teaches that the gate insulating film have silicon oxide film) formed on said silicon substrate so as to be in contact therewith, and said nitrogen containing high-dielectric-constant insulating film (the nitrogen-containing HfO2 film) formed on said silicon oxide film so as to be in contact therewith.

With respect to claim 27, Cho discloses wherein said silicon substrate (again, there is nitrogen only at the top of the HfO2 film, just like the nitrogen concentration distribution in the applicant's Fig. 1 layer 103) and said gate insulating film (the nitrogen-containing HfO2 film) are in contact with each other, and said gate insulating film (the nitrogen-containing HfO2 film) and a gate electrode (the TaN or poly-Si film) are in contact with each other; and said gate electrode is made of either a polysilicon or a polysilicon germanium conductive film (the TaN or poly-Si film).

With respect to claim 28, Cho discloses wherein said gate insulating film contains at least one type selected from the group consisting of Zr, Hf, Ta, A1, Ti, Nb, Sc, Y, La,

Ce, Pr, Nd, Sm, Eu, Gd, Tb. Dy, Ho, Er, Tm, Yb and Lu (the nitrogen-containing HfO2 film).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (the article titled "Novel Nitrogen Profile Engineering for Improved TaN/HfO2/Si MOSFET Performance" submitted in the Information Disclosure Statement filed on December 23, 2004).

With respect to claim 25, Cho discloses wherein the nitrogen concentration on a silicon substrate (again, there is nitrogen only at the top of the HfO2 film, just like the nitrogen concentration distribution in the applicant's Fig. 1 layer 103) side interface of said gate insulating film (the nitrogen-containing HfO2 film) is less than 3 atomic %.

Cho did not discloses the insulating film is less than 3 atomic %, however, it is well settled that "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) (Claimed process which was performed at a temperature between 40-80 C degree and an acid concentration between 25%-70% was held to be prima facie obvious over a reference process which differed from the claims only in that the reference process was performed

at a temperature of 100 C degree and an acid concentration of 10%.); see also Peterson, 315 F.3d at 1330, 65 USPQ2d at 1382 ("normal desire of scientists or artisans to improve upon what is already generally known provides the motivation to determine where in disclosed set of percentage ranges is the optimum combination of percentages.").

Allowable Subject Matter

Claims 29-39 are allowed.

Claim 29 is allowable over the reference of record because none of these references disclose or can be combined to yield the claimed invention of a semiconductor device stacked a gate with gate insulating film comprises a nitrogen containing high-dielectric-constant insulating film a position at which the nitrogen concentration in said nitrogen containing high-dielectric-constant insulating film selectively bonds with a silicon atom in metal silicate.

Claim 34 is allowable over the reference of record because none of these references disclose or can be combined to yield the claimed invention of a semiconductor device stacked a gate with gate insulating film comprises a nitrogen containing high-dielectric-constant insulating film nitrogen is introduced only into a region lying between the position at which the silicon concentration has the minimum value and said gate electrode side interface.

Claim 37 is allowable over the reference of record because none of these references disclose or can be combined to yield the claimed invention of a semiconductor device a gate insulating film and a gate electrode stacked in this order,

wherein said gate insulating film and said gate electrode are in contact with each other; wherein said gate insulating film has a layered structure having, from the silicon substrate side, a first silicon oxide film, a metal oxide film or a metal silicate film, and a second silicon oxide film stacked in this order; wherein only the second silicon oxide film has a structure in which nitrogen is introduced into silicon oxide; wherein the first silicon oxide film, the metal oxide film and the metal silicate film do not contain nitrogen.

Claims 30-33, 35,36, 38 and 39 contain allowable subject matter by virtue of their dependency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

/Tsz K Chiu/
Examiner, Art Unit 2822